IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Kevin J. Ryan
Title: PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS
Attorney Docket No.: 303.306US2

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
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We are transmitting herewith the following attached items and information (as indicated with an "X"):

X **DIVISIONAL** of prior Patent Application No. 08/886,753 (under 37 CFR § 1.53(b)) comprising:
- X Specification (27 pgs, including claims numbered 1 through 31 and a 1 page Abstract).
- X Formal Drawing(s) (5 sheets).
- X Copy of signed Combined Declaration and Power of Attorney (3 pgs) from prior application.
- X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
- X Check in the amount of $1,678.00 to pay the filing fee.

X Prior application is assigned of record to Micron Technology, Inc..
X Information Disclosure Statement (1 pgs), Form 1449 (1 pgs). References NOT enclosed, cited in prior application.
X Preliminary Amendment (11 pgs).
X Return postcard.

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INDEPENDENT CLAIMS	12 - 3 =	9	x 78 =	$702.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
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Applicant:	Kevin J. Ryan	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.306US2
Title:	PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Before taking up the above-identified application for examination, please enter the following amendments.

IN THE SPECIFICATION

In the first line after the title, please insert the following --This application is a Divisional of U.S. Application No. 08/886,753, filed July 1, 1997.--

IN THE CLAIMS

Please cancel claims 1-4 and 9-28 without prejudice, amend claims 5, 6, and 29-31, and add new claims 32-56 as follows:

5. (Amended) A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices <u>wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder</u>;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

6. (Amended) The memory system according to claim 5, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of one of the plurality of pipelined memory subsystems and a second delay introduced by the data register of one of the plurality of pipelined memory subsystems.

29. (Amended) A method [for] of retrieving data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising [the steps of]:

issuing commands and addresses on a unidirectional command and address bus;

latching the commands and addresses in the [a plurality of] buffer registers;

driving the latched commands and addresses to the column and row decoders [a plurality of memory devices having addressable storage];

retrieving [the] data from the addressable storage of one of the plurality of memory devices;

latching the data in [a] the data registers; and

receiving the data on a bidirectional data bus.

30. (Amended) The [memory system] method of retrieving data according to claim 29 wherein each of the memory devices is a dynamic random access memory device.

31. (Amended) The method of [storing information] retrieving data in a pipelined memory system according to claim 29 wherein [the step of communicating] issuing commands and addresses and [the step of communicating] receiving data communicates according to a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

32. (New) A method of storing data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses in the plurality of buffer registers;

latching the data in the plurality of data registers;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of the plurality of memory devices.

33. (New) The method of claim 32, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the buffer register of one of the plurality of memory subsystems and a second delay introduced by the data register of one of the plurality of memory subsystems.

34. (New) An electronic system comprising:

a microprocessor;

a memory controller coupled to the microprocessor;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

35. (New) The electronic system of claim 34, wherein the memory controller communicates the commands and addresses and data information using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of one of the plurality of pipelined memory subsystems and a second delay introduced by the data register of one of the plurality of pipelined memory subsystems.

36. (New) The electronic system of claim 34, wherein each memory device is a dynamic random access memory device.

37. (New) The electronic system of claim 34, wherein both M and N equal eight.

38. (New) A method of performing a memory transaction in an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller;

issuing commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses received from the unidirectional command and address bus in the buffer registers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices; and

if the memory transaction is a write, receiving and latching the data in the data registers of the plurality of memory subsystems and driving the latched data to the plurality of memory devices.

39. (New) The method of claim 38, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

40. (New) A method of storing data, in an electronic system, having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses read from the unidirectional command and address bus in the buffer registers of the plurality of memory subsystems;

latching the data received from the bidirectional data bus in the data registers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices;

driving the latched data to the plurality of memory devices; and

storing the data in addressable storage of the plurality of memory devices.

41. (New) The method of claim 40, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

42. (New) In an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, a method of retrieving data comprising:

issuing information to the memory controller;

issuing commands and addresses on a unidirectional command and address bus;

latching the commands and addresses read from the unidirectional command and address bus in the buffer registers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices of the plurality of memory subsystems;

retrieving data from addressable storage of the plurality of memory devices of the plurality of memory subsystems;

latching the data in the data register of the plurality of memory devices of the plurality of memory subsystems; and

receiving the data on a bidirectional data bus.

43. (New) The method of claim 42, wherein issuing commands and addresses and receiving data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

44. (New) A memory system comprising:

a unidirectional command and address bus coupleable to a memory control device;

a bidirectional data bus coupleable to the memory control device; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

45. (New) The memory system of claim 44, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of one of the plurality of pipelined memory subsystems and a

second delay introduced by the data register of one of the plurality of pipelined memory subsystems.

46. (New) The memory system of claim 44, wherein each memory device is a dynamic random access memory device.

47. (New) The memory system of claim 44, wherein both M and N equal eight.

48. (New) A method of storing data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

receiving commands and addresses from a unidirectional command and address bus;
receiving data from a bidirectional data bus;
latching the commands and addresses in the plurality of buffer registers;
latching the data in the plurality of data registers;
driving the latched commands and addresses to the column and row decoders;
driving the latched data to the data in buffers; and
storing the data in the addressable storage of the plurality of memory devices.

49. (New) The method of claim 48, wherein receiving commands and addresses and receiving data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

50. (New) A method of retrieving data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

receiving commands and addresses from a unidirectional command and address bus;
latching the commands and addresses in the plurality of buffer registers;
driving the latched commands and addresses to the column and row decoders;
retrieving data from the addressable storage of the plurality of memory devices;
latching the data in the plurality of data registers; and
driving the data onto a data bus.

51. (New) The method of claim 50, wherein receiving commands and addresses and driving the data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

52. (New) A memory system, comprising:

a unidirectional command and address bus in electrical communication with a memory control device;

a bidirectional data bus in electrical communication with the memory control device; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from

the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

53. (New) The memory system of claim 52, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of one of the plurality of pipelined memory subsystems and a second delay introduced by the data register of one of the plurality of pipelined memory subsystems.

54. (New) The memory system of claim 52, wherein each memory device is a dynamic memory device.

55. (New) The memory system of claim 52, wherein both N and M equal eight.

56. (New) A method of retrieving data in a pipelined memory system, comprising:

issuing commands and addresses on a unidirectional command and address bus to a plurality of memory subsystems;

latching the commands and addresses in a buffer register in each of the plurality of memory subsystems;

driving the latched commands and addresses to column and row decoders in each of the plurality of subsystems;

retrieving data from addressable storage of one of the plurality of memory subsystems;

latching the data in a data register of the one of the plurality of memory subsystems; and

receiving the data on a bidirectional data bus.

CONCLUSION

Claims 1-4 and 9-28 have been canceled without prejudice and not in response to an art rejection. Applicant reserves the right to reintroduce these claims at a later date or in a continuation or divisional patent application. Claims 5, 6, and 29-31 have not been amended in response to any art rejection. New claims 32-56 are drawn to control of pipelined memories and fit within Group II of the Restriction Requirement of the parent case.

Claims 5-8 and 29-56 are now pending in this application. The Examiner is invited to contact the below-signed attorney to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

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By their Representatives,

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PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS

Field of the Invention

This invention relates generally to the field of memory devices, and more particularly to a pipelined packet-oriented synchronous DRAM interface.

Background of the Prior Art

Conventional memory devices have a standard interface consisting of separate address, data and control pins. For example, one version of a synchronous dynamic random access memory (SDRAM) has twelve address pins, two multiplexed address and control pins, seven control pins and sixteen data pins. This approach offers a great deal of flexibility since computer systems vary greatly in their memory requirements. In particular, the bandwidth of memory systems using SDRAMs can easily be increased by adding another SDRAM in parallel to the existing SDRAMs, thereby increasing the width of the memory bus.

The tradeoff for this flexibility is, however, an increase in layout space which leads to an increase in manufacturing cost. Separate traces need to be run for each pin of each SDRAM. Therefore, it is sometimes cost prohibitive to use SDRAMS for wide memory systems.

One approach to lower the cost of expanding memory is to use memory devices which multiplex address, control and data information on the same pins. For example, some memory devices have a set of generic interface pins which connect to a high-speed, synchronous bus. Communication over the bus is accomplished by a series of packets which conform to a predefined packet protocol. Usually the packet protocol is fairly sophisticated and has a complete command set. For example, DRAMS conforming to the RAMBUS™ interface communicate using a protocol in which each packet consists of six bytes transmitted sequentially over a high-speed bus known as a "Channel." In this manner, the packets encapsulate all address, control and data information.

Because of the efficient use of generic interface pins, a packet protocol reduces the required number of pins to approximately 30. However, this has the disadvantage of decreasing effective data bandwidth, because only a portion of the total bus bandwidth is available for data (the rest of the bandwidth is reserved for address and control information).

Another method for reducing the cost associated with increasing total memory bandwidth, without decreasing effective data bandwidth, is to provide a second high-speed bus specifically for communicating data. In this approach, address and control information is communicated over a unidirectional high-speed address/control bus while data is communicated over a bidirectional high-speed data bus. Both communications conform to a predefined packet protocol. This approach has the benefits of reducing the total pin count (although not as much as the RAMBUS™ protocol described above), yet has the added benefit that only the data bus needs to be duplicated when the width of the memory system is increased.

Both approaches described above offer advantages over traditional memory architectures in terms of increased data retrieval bandwidth. It is difficult, however, to implement systems having both fine granularity and large memory depth using such devices. What is needed is a memory architecture which supports increased bandwidth, fine granularity, and large memory arrays.

Summary of the Invention

As explained in detail below, an improved memory system is provided having a unidirectional command and address bus coupled to a memory controller, the memory controller communicating commands and addresses to the command and address bus. A bidirectional data bus is also coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation. The memory system further includes a plurality of memory devices, a buffer register connected between the command and address bus

and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, and a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

In another embodiment of the invention, the memory system has a unidirectional command and address bus coupled to a memory controller, the memory controller communicating commands and addresses to the command and address bus, and a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation. The memory system further includes a plurality of pipelined memory subsystems, each memory subsystem having a plurality of memory devices, a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, and a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

According to another feature of the invention, the memory system includes a unidirectional command and address bus coupled to a memory controller, the

memory controller communicating commands and addresses to the command and address bus, and a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation. The memory system further includes a memory module including a pipelined memory subsystem. The pipelined memory subsystem includes: a) a plurality of memory devices, b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, and c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation. The memory system also has a socket adapted to receive the memory module and to couple the pipelined memory subsystem of the memory module to the unidirectional command and address bus and to the bidirectional data bus.

In order to solve the problems in the prior art, we have provided a method for storing data in a pipelined memory system. The method includes the steps of communicating commands and addresses to a unidirectional command and address bus, communicating data information to a bidirectional data bus, latching the commands and addresses in a plurality of buffer registers, latching the data in a plurality of data registers, driving the latched commands and addresses to a plurality of memory devices having addressable storage, driving the latched data to the plurality of memory devices, and storing the data in the addressable storage of one of the plurality of memory devices.

These and other features and advantages of the invention will become apparent from the following description of the preferred embodiments of the invention.

Brief Description of the Drawing

Figure 1 is a block diagram of one embodiment of a packet-oriented memory system having a command/address bus, a data bus and a plurality of pipelined memory subsystems;

Figure 2 is a block diagram of an alternate embodiment of a packet-oriented memory system having a single C/A bus, two data busses and a first and second plurality of pipelined memory subsystems;

Figure 3 is a block diagram of one embodiment of a memory system having a plurality of memory modules where each memory module has a single pipelined memory subsystem;

Figure 4 is a block diagram of an alternate embodiment of a memory system having a plurality of memory modules where each memory module includes a plurality of pipelined memory subsystems; and

Figure 5 is a block diagram of an alternate embodiment of a memory system having a plurality of memory modules coupled to a first and second data bus, each memory module having two memory subsystems.

Description of the Present Invention

In the following detailed description, references are made to the accompanying drawings which illustrate specific embodiments in which the invention may be practiced. Electrical, mechanical, logical and structural changes may be made to the embodiments without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense and the scope of the present invention is defined by the appended claims and their equivalents.

In a memory system having a single high-speed command and address bus (C/A bus) and a high-speed data bus, the C/A bus will experience the same electrical loading as the high-speed data bus. Assuming similar physical layouts for each bus, a maximum frequency of operation is similar for each bus and is primarily determined by the number of devices on the bus.

In order to increase the bandwidth of a memory system having two high-speed busses, a new memory device is added in parallel to the existing devices and a corresponding data bus is added. For example, assume that a memory system has a single memory device, a single C/A bus and a single data bus. In order to increase the bandwidth of the memory system a second memory device may be added in parallel to the first. In this manner, the memory system uses a single C/A bus and two data busses. Since each memory device has its own data bus, the effective bandwidth of the system is doubled.

At the same time, however, loading on the single C/A bus also doubles. In fact, as the bandwidth of a memory system is increased, the loading on the C/A bus increases at a rate directly proportional to that increase. As the number of devices on a bus increases, the frequency at which the bus can be reliably operated therefore decreases. Thus, in increased bandwidth implementations, the maximum frequency of operation for the C/A bus will be lower than that for the data bus. Since both busses are typically run at the same frequency, the bandwidth of the memory system is limited by the number of devices on the C/A bus. Similarly, at a given operating frequency, there is a maximum number of devices that can be supported on the C/A bus, and hence in the memory system.

Conventional microprocessor based systems utilize three busses: a memory data bus, a command bus and an address bus. For example, one popular Intel microprocessor based system provides a 66 MHz memory data bus, a 66 MHz command bus and a 66 MHz address bus. Each of the command and address busses is capable of driving up to 64 loads. The data bus can only drive eight loads. At a clock speed of 66 MHz and a data width of 64 bits, such a system has a bandwidth

of approximately .5 GBytes/second. It is desirable, however, to substantially increase this bandwidth to the order of 1.6 GBytes/s. If a single 16-bit data bus is used, it must be operated at approximately 800 MHz in order to achieve the desired data rate. It is also desirable to continue to support 64 devices; however, simulations demonstrate that, with improvements to the signaling and physical environment, the number of loads that can be supported at a data rate of 800 MHz is approximately eight. In order to support 64 devices in a system with eight devices per 16-bit data bus, eight data busses would be required. This results in a 128-bit wide data path. Such a wide data path is inconsistent with the desire to reduce the total number of traces and is cost prohibitive.

The present invention is a system which uses a unidirectional C/A bus and a data bus yet supports a plurality of devices per bus such that the total width of the data path width is not cost prohibitive to manufacture. For example, the present invention provides a memory system which utilizes a single 16-bit data bus which can be operated at 800 MHz and which supports 64 devices. Such a system can also be implemented as a higher bandwidth multiple data bus system as is described below.

Figure 1 is a block diagram of one embodiment of a packet-oriented memory system according to the present invention. Referring to Figure 1, memory system 100 includes a memory controller 105, a command/address bus (C/A) bus 110, a data bus 115 and a plurality of pipelined memory subsystems 130.1 through 130.N, where N is the number of subsystems in memory system 100. Memory controller 105 communicates commands and addresses to C/A bus 110. Furthermore, memory controller 105 is coupled to data bus 115 for reading and writing data from memory subsystems 130 thereon. In one embodiment, C/A bus 110 is a unidirectional high-speed bus while data bus 115 is a bidirectional high-speed bus. Memory controller 105 communicates data information to data bus 110 during a write cycle and receives data information from data bus 115 during a read cycle. Memory controller

105 communicates over C/A bus 110 and data bus 115 via a predetermined packet protocol.

Each memory subsystem 130 includes a C/A buffer register 131, a plurality M of memory devices 135 and a data buffer register 141. C/A buffer register 131 receives and latches the command and address information from C/A bus 110. As illustrated in Figure 1, buffer register 131 is connected between the command and address bus 110 and the plurality of memory devices 135.1 through 135.M. In one embodiment, memory system 100 has eight memory subsystems and eight memory devices 135 (i.e. N plus M equals eight). In another embodiment, memory devices 135 are dynamic random access memory devices (DRAMs). The number of memory devices 135 connected to each buffer register 131 may, however, differ from that shown in memory system 100 without departing from the spirit of the present invention.

As illustrated, memory system 100 comprises N C/A registers 131 and N*M DRAMs. Each register drives the latched command and address information to its corresponding plurality of memory devices. In this manner, the load on the C/A bus is reduced from N*M devices to only N devices.

Each data register 141 is connected between the plurality of memory devices 135 and data bus 115. For memory read operations, data registers 141 receive and latch data information from memory devices 135. Upon the next clock cycle, data registers 141 provide the information to memory controller 105 by driving the data information on data bus 115. For memory write operations, each data register 141 receives and latches data information from data bus 120. Upon the next clock cycle, data registers 141 drive the data information to their corresponding M memory devices 135. In this manner, the load on data bus 120 is reduced from N*M devices to only N devices.

Each C/A buffer register 131, its corresponding plurality of memory devices 135.1 through 135.M and its corresponding data register 141 define a pipelined memory subsystem 130. Memory subsystems 130.1 through 130.N allow C/A bus

110 and data bus 120 to operate at a significant higher data rate since the loading was reduced by a factor of M. Pipelined memory subsystems 130, however, add a two clock cycle delay to DRAM access. In order to ensure efficient operation, the packet protocol used for communication is defined to incorporate a first delay for C/A buffer register 131 and a second delay for data register 141. Furthermore, memory controller 105 issues command and address packets and data packets in pipeline fashion such that the first delay and the second delay do not have a substantial impact on the performance of memory system 100.

Figure 2 is a block diagram of an alternate embodiment of a packet-oriented memory system having pipelined memory subsystems. Referring to Figure 2, memory system 200 includes a memory controller 205, a command/address bus (C/A) bus 210, a first data bus 215, a second data bus 217, a first plurality of pipelined memory subsystems 230.1 through 230.N and a second plurality of pipelined memory subsystems 240.1 through 240.P. In this configuration, N and P are the number of pipelined memory subsystems in the first and second plurality of pipelined memory subsystems, respectively.

Memory controller 205 communicates commands and addresses to C/A bus 210. Memory controller 205 is coupled to a first data bus 215 and a second data bus 217. C/A bus 210 is a unidirectional high-speed bus while data busses 215 and 217 are bidirectional high-speed busses. Memory controller 205 communicates data information to data busses 215 and 217 during a memory write cycle and receives data information from data busses 215 and 217 during a read cycle. Memory controller 205 communicates over C/A bus 210 and data busses 215 and 217 via a predetermined packet protocol.

Each of the first plurality of pipelined memory subsystems 230.1 through 230.N includes a C/A buffer register 231, a plurality M of memory devices 235 and a data buffer register 241. Similarly, each of the second plurality of pipelined memory subsystems 240.1 through 240.P includes a C/A buffer register 231, a plurality M of memory devices 235 and a data buffer register 241.

C/A buffer register 231 receives and latches the command and address information from C/A bus 210. In the first plurality N of pipelined memory subsystems, register 231 is connected between the command and address bus 210 and a plurality of memory devices 235.1 through 235.M. In the second plurality P of pipelined memory subsystems, register 231 is connected between the command and address bus 210 and a plurality of memory devices 235.1 through 235.Q. In one embodiment, the number of memory subsystems N and the number of memory subsystems P is four and eight dynamic random access memory devices (DRAMs) 235 are connected to each register 231 (i.e. N=4, P=4, M=8 and Q=8).

Data registers 241 of memory subsystems 230 are connected between the plurality M of memory devices 235 and the first bidirectional data bus 215. Similarly, data registers 241 of memory subsystems 240 are connected between the plurality Q of memory devices 235 and the second bidirectional data bus 217. For memory read operations, data registers 241 receive and latch data information from the corresponding plurality of DRAMs 235. Upon the next clock cycle, data registers 241 drive the data information to corresponding data busses 215 and 217. For memory write operations, data registers 241 receive and latch data information from corresponding data busses 215 and 217 and drive the data information to the plurality of memory devices 235.

As illustrated in Figure 2, memory system 200 has N+P C/A buffer registers 231 and (N*M) + (P*Q) memory devices 235. In this manner, the load on the C/A bus is reduces from (N*M) + (P*Q) devices to N+P devices. Similarly, the load on data busses 215 and 217 is reduced from N*M and P*Q devices to N and P devices, respectively. The maximum data bandwidth of memory system 200 is thereby directly increased. As described earlier, pipelined memory subsystems 230 and 240 adds a two clock cycle delay to DRAM access. Memory controller 205 issues command and address packets and data packets in a pipelined fashion in order to optimize communication throughput such that the first delay and the second delay do not have a substantial impact on the performance of memory system 200.

Figure 3 is a block diagram of one embodiment of a memory system having a plurality of memory modules, each memory module having a single pipelined memory subsystem. Referring to Figure 3, memory system 300 includes memory controller 305, a C/A bus 310, a data bus 315, a plurality R of memory modules 320 and a plurality of sockets (not shown). Memory controller 305 communicates commands and addresses to C/A bus 310. Furthermore, memory controller 305 is coupled to data bus 315. C/A bus 310 is a unidirectional high-speed bus while data bus 315 is a bidirectional high-speed bus. Memory controller 305 communicates data information to data bus 315 during a write cycle and receives data information from data bus 315 during a read cycle. Memory controller 305 communicates over C/A bus 310 and data bus 315 via a predetermined packet protocol.

Each memory module 320 represents any physical device which encapsulates at least one memory subsystem. In one embodiment, a memory module may be a single in-line memory module (SIMM). In order to provide for flexible configuration, memory system 300 has a plurality of sockets (not shown) which are adapted to receive memory modules. The plurality of sockets are disposed between each memory module 320 and C/A bus 310 and data bus 315 such that a socket receives a memory module 320 and couples memory module 320 to C/A bus 310 and data bus 315. Thus, the sockets allow memory modules 320 to easily be added to or removed from memory system 300.

Each memory module 320 has at least one pipelined memory subsystem. For purposes of illustration, memory module 320.1 is shown with a single pipelined memory subsystem 330. Memory subsystem 330 comprises C/A buffer register 331, a plurality M of memory devices 335 and a data buffer 341. C/A buffer register 331 is coupled between C/A bus 310 and the plurality M of memory devices 335.1 through 335.M. C/A buffer register 331 receives and latches the command and address information from C/A bus 310. Data register 341 is connected between data bus 315 and the plurality M of memory modules 335. For memory read operations, data register 341 receives and latches data information from the plurality

of memory devices 335 and drives the data information to data bus 320. For memory write operations, data register 341 receives and latches data information from data bus 320 and drives the data information to the plurality of memory devices. In this manner, the load on C/A bus 310 and data bus 320 is reduced from R*M devices to R devices, thereby allowing C/A bus 310 and data bus 320 to achieve higher operating speeds.

Figure 4 is a block diagram of an alternate embodiment of a memory system having a plurality of memory modules, each memory module having a plurality of pipelined memory subsystems. More specifically, memory system 400 includes memory controller 405, a C/A bus 410, a data bus 415, a plurality R of memory modules 420 and a pluralityof sockets (not shown). Memory controller 405 communicates commands and addresses to C/A bus 410. Furthermore, memory controller 405 is coupled to data bus 415 for reading and writing data from memory subsystems 430. In one embodiment, C/A bus 410 is a unidirectional high-speed bus while data bus 415 is a bidirectional high-speed bus. Memory controller 405 communicates data information to data bus 415 during a memory write cycle and receives data information from data bus 415 during a read cycle. Memory controller 405 communicates over C/A bus 410 and data bus 415 via a predetermined packet protocol.

Each memory module 420 of memory system 400 includes a plurality N of pipelined memory subsystems 430.1 through 430.N. Furthermore, each memory subsystem 430 include a C/A buffer register 431, a plurality M of memory devices 435.1 through 435.M, and a data buffer 441. C/A buffer register 431 is coupled between C/A bus 410 and the plurality of memory devices 435. C/A buffer register 431 receives and latches the command and address information from C/A bus 410. Data register 441 is connected between data bus 415 and the plurality of memory modules 435. For memory read operations, data register 441 receives and latches data information from the plurality of memory devices 435 and drives the data information to data bus 415. For memory write operations, data register 441

receives and latches data information from data bus 415 and drives the data information to the plurality of memory devices 435. In this manner, the load on data bus 415 is reduced by a factor of M.

Figure 5 is a block diagram of an alternate embodiment of a memory system having a plurality of memory modules coupled to two data busses, each memory module having two memory subsystems. Memory system 500 is similar to memory system 400 illustrated in Figure 4 except that memory system 500 implements a wider data path.

Memory system 500 includes memory controller 505, C/A bus 510, a first data bus 515, a second data bus 517, a pluralityof sockets (not shown) and a plurality R of memory modules 520. Each memory module 520.1 through 520.R includes a first and second memory subsystem 530.1 and 530.2. Memory subsystems 530 include a C/A buffer register 531, a plurality M of memory devices 535 and a data register 541. In one embodiment, memory system 500 has four sockets (not shown), four memory modules 520, each memory module 520 having two memory subsystems 530 of eight memory devices 535 (i.e., R=4 and M=8). In another embodiment, the memory devices 535 are SDRAMs.

Memory controller 505 communicates commands and addresses to C/A bus 510. Memory controller 505 is coupled to data busses 515 and 517. In one embodiment, C/A bus 510 is a unidirectional high-speed bus while data busses 515 and 517 are bidirectional high-speed busses. Memory controller 505 communicates data information to data busses 515 and 517 during a memory write cycle and receives data information from data busses 515 and 517 during a read cycle. Memory controller 505 communicates over C/A bus 510 and data busses 515 and 517 via a predetermined packet protocol.

Buffer register 531 of pipelined memory subsystems 530 receive and latch the command and address information from C/A bus 410. Data register 541 of memory subsystem 530.1 is connected between data bus 515 and the plurality of memory devices 535. Data register 542 of memory subsystem 530.1, however, is

connected between data bus 517 and its corresponding plurality of memory modules 535. In this manner, memory system 500 has a wider data path than memory system 400 of Figure 4.

For memory read operations, data register 541 of memory subsystem 530.1 receives and latches a first data information from its corresponding plurality of memory devices 535 and drives the first data information to data bus 515. Similarly, during a read operation, data register 541 of memory subsystem 530.2 receives and latches a second data information from its corresponding plurality of memory devices 535 and drives the second data information to data bus 517. For memory write operations, data register 541 of memory subsystem 530.1 receives and latches the first data information from data bus 515 and drives the first data information to its corresponding plurality of memory devices 535. Similarly, data register 541 of memory subsystem 530.2 receives and latches the second data information from data bus 520 and drives the second data information to its corresponding plurality of memory devices 535. In this manner, the loads C/A bus 510 and on both data busses 515 and 517 are reduced from M*R devices to R devices.

Conclusion

Various embodiments of a pipelined, packet-oriented memory systems have been described. Such a system offers the flexibility of multiple busses having a plurality of memory devices yet allows the busses to operate at a high data rate. In one embodiment, the memory system comprises a plurality of memory subsystems coupled to a high-speed command and address bus and a high-speed data bus, each memory subsystem having eight memory devices. In another embodiment, a first plurality of pipelined memory subsystems uses a first data bus while a second plurality of pipelined memory subsystems uses a second data bus. In another embodiment, the memory system has a plurality of sockets adapted to receive a memory module, wherein a memory module contains at least one memory

subsystem. In another embodiment, the memory system has a first plurality of sockets connected to a first data bus and a second plurality of sockets connected to a second data bus, the memory modules comprising two memory subsystems. This application is intended to cover any adaptations or variations of the present invention. It is manifestly intended that this invention be limited only by the claims and equivalents thereof.

What is claimed is:

1. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a plurality M of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

2. The memory system according to claim 1 wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

3. The memory system according to claim 1 wherein each memory device is a dynamic random access memory device.

4. The memory system according to claim 1 wherein M equals 8.

5. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

6. The memory system according to claim 5 wherein the memory controller communicates the commands and addresses using a pipelined packet-protocol which

incorporates a first delay introduced by the buffer register of the plurality of pipelined memory subsystems and a second delay introduced by the data register of the plurality of pipelined memory subsystems.

7. The memory system according to claim 5 wherein each memory device is a dynamic random access memory device.

8. The memory system according to claim 5 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein N equals eight.

9. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a first bidirectional data bus coupled to the memory controller, the memory controller communicating first data information to the bidirectional data bus for a write operation and receiving the first data information from the bidirectional data bus during a read operation;

a second bidirectional data bus coupled to the memory controller, the memory controller communicating second data information to the second bidirectional data bus for a write operation and receiving the second data information from the second bidirectional data bus during a read operation;

a first plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and

latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the first bidirectional data bus, the data register receiving and latching the first data information from the first bidirectional data bus and driving the first data information to the plurality of memory devices for a write operation, the data register receiving and latching the first data information from the plurality of memory devices and driving the first data information to the first bidirectional data bus for a read operation; and

a second plurality P of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the second bidirectional data bus, the data register receiving and latching the second data information from the second bidirectional data bus and driving the second data information to the plurality of memory devices for a write operation, the data register receiving and latching the second data information from the plurality of memory devices and driving the second data information to the bidirectional data bus for a read operation.

10. The memory system according to claim 9 wherein the memory controller communicates the commands and addresses using a pipelined packet protocol which incorporates a first delay introduced by the buffer register of the first plurality of

pipelined memory subsystems and by the buffer register of the second plurality of pipelined memory subsystems, and a second delay introduced by the data register of the first plurality of pipelined memory subsystems and by the data register of the second plurality of pipelined memory subsystems.

11. The memory system according to claim 9 wherein each memory device of the first plurality of pipelined memory subsystems and each memory device of the second plurality of pipelined memory subsystems is a dynamic random access memory device.

12. The memory system according to claim 9 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and each of the plurality P of pipelined memory subsystems include eight memory devices and further wherein N and P equal 4.

13. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a memory module wherein each pipelined memory subsystem includes:

a plurality M of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus

and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus.

14. The memory system according to claim 13 wherein the memory controller communicates the commands and addresses using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of the memory subsystem and a second delay introduced by the data register of the memory subsystem.

15. The memory system according to claim 13 wherein each memory device is a dynamic random access memory device.

16. The memory system according to claim 13 wherein M equals 8.

17. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a plurality R of memory modules wherein at each memory module includes a plurality N of pipelined memory subsystems including:

a plurality of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices;

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a plurality of sockets, wherein each socket is adapted to receive one of the R memory modules and to couple the received memory module to the unidirectional command and address bus and to the bidirectional data bus.

18. The memory system according to claim 17 wherein the memory controller communicates the commands and addresses using a pipelined packet protocol which incorporates a first delay introduced by the buffer register of the memory subsystem and a second delay introduced by the data register of the memory subsystem.

19. The memory system according to claim 17 wherein each memory device is a dynamic random access memory device.

20. The memory system according to claim 17 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein the number of sockets equals eight, R equals eight and N equals one.

21. The memory system according to claim 17 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein the number of sockets equals four, R equals four and N equals two.

22. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a first bidirectional data bus coupled to the memory controller, the memory controller communicating first data information to the bidirectional data bus for a write operation and receiving the first data information from the bidirectional data bus during a read operation;

a second bidirectional data bus coupled to the memory controller, the memory controller communicating second data information to the second bidirectional data bus for a write operation and receiving the second data information from the second bidirectional data bus during a read operation;

a first and second memory module, the first and second memory module each having a first memory subsystem and a second memory subsystem; and

a first and second socket, the first socket adapted to receive the first memory module and to couple the first memory module to the unidirectional command and address bus and to the first bidirectional data bus, the second socket adapted to receive the second memory module and to couple the second memory module to the unidirectional command and address bus and to the second bidirectional data bus.

23. The memory system according to claim 22 wherein the first memory subsystem comprises:

a) a plurality of memory devices;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the first bidirectional data bus, the data register receiving and latching the first data information from the first bidirectional data bus and driving the first data information to the plurality of memory devices for a write operation, the data register receiving and latching the first data information from the plurality of memory devices and driving the first data information to the first bidirectional data bus for a read operation, and further wherein the second memory subsystem includes:

i) a plurality of memory devices;

ii) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

iii) a data register connected between the plurality of memory devices and the second bidirectional data bus, the data register receiving and latching the second data information from the second bidirectional data bus and driving the second data information to the plurality of memory devices for a write operation, the data register receiving and latching the second data information from the

plurality of memory devices and driving the second data information to the bidirectional data bus for a read operation.

24. The memory system according to claim 23 wherein the memory controller communicates the commands and addresses using a pipelined packet protocol which incorporates a first delay introduced by the buffer register of the first memory subsystem and by the buffer register of the second memory subsystem and a second delay introduced by the data register of the first memory subsystem and by the data register of the second memory subsystem.

25. The memory system according to claim 23 wherein each memory device of the first memory subsystem and each memory device of the second memory subsystem is a dynamic random access memory device.

26. A method for storing data in a pipelined memory system, comprising the steps of:

communicating commands and addresses to a unidirectional command and address bus;

communicating data information to a bidirectional data bus;

latching the commands and addresses in a plurality of buffer registers;

latching the data in a plurality of data registers;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

driving the latched data to the plurality of memory devices; and

storing the data in the addressable storage of one of the plurality of memory devices.

27. The method of storing information in a pipelined memory system according to claim 26 wherein the step of communicating commands and addresses and the

step of communicating data communicates according to a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

28. The method of storing information in a pipelined memory system according to claim 26 wherein each of the memory devices is a dynamic random access memory device.

29. A method for retrieving data in a pipelined memory system, comprising the steps of:

issuing commands and addresses on a unidirectional command and address bus;

latching the commands and addresses in a plurality of buffer registers;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

retrieving the data from the addressable storage of one of the plurality of memory devices;

latching the data in a data register; and

receiving the data on a bidirectional data bus.

30. The memory system according to claim 29 wherein each of the memory devices is dynamic random access memory device.

31. The method of storing information in a pipelined memory system according to claim 29 wherein the step of communicating commands and addresses and the step of communicating data communicates according to a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

Abstract of the Disclosure

A memory system having at least one memory subsystem and using a packet protocol communicated over a command and address bus and at least one data bus. The memory subsystems are pipelined to achieve wide data paths and to support a high number of memory devices, such as dynamic random access memory devices, per data bus. The packet protocol is defined to compensate for the delay stages of the pipelined memory subsystem in order to optimize the access time of the memory devices.

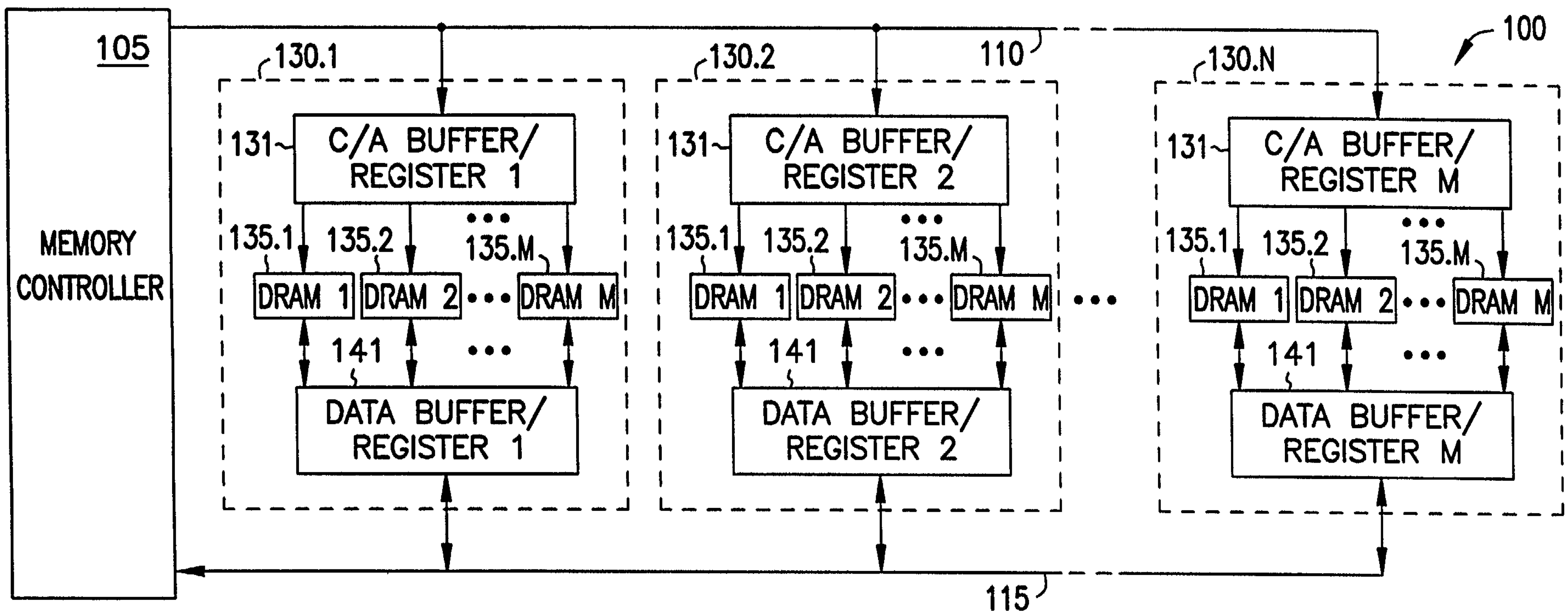
105
MEMORY
CONTROLLER
100
110
115
130.1
130.2
130.N
131
C/A BUFFER/
REGISTER 1
C/A BUFFER/
REGISTER 2
C/A BUFFER/
REGISTER M
135.1
135.2
135.M
DRAM 1
DRAM 2
DRAM M
141
DATA BUFFER/
REGISTER 1
DATA BUFFER/
REGISTER 2
DATA BUFFER/
REGISTER M

FIG. 1

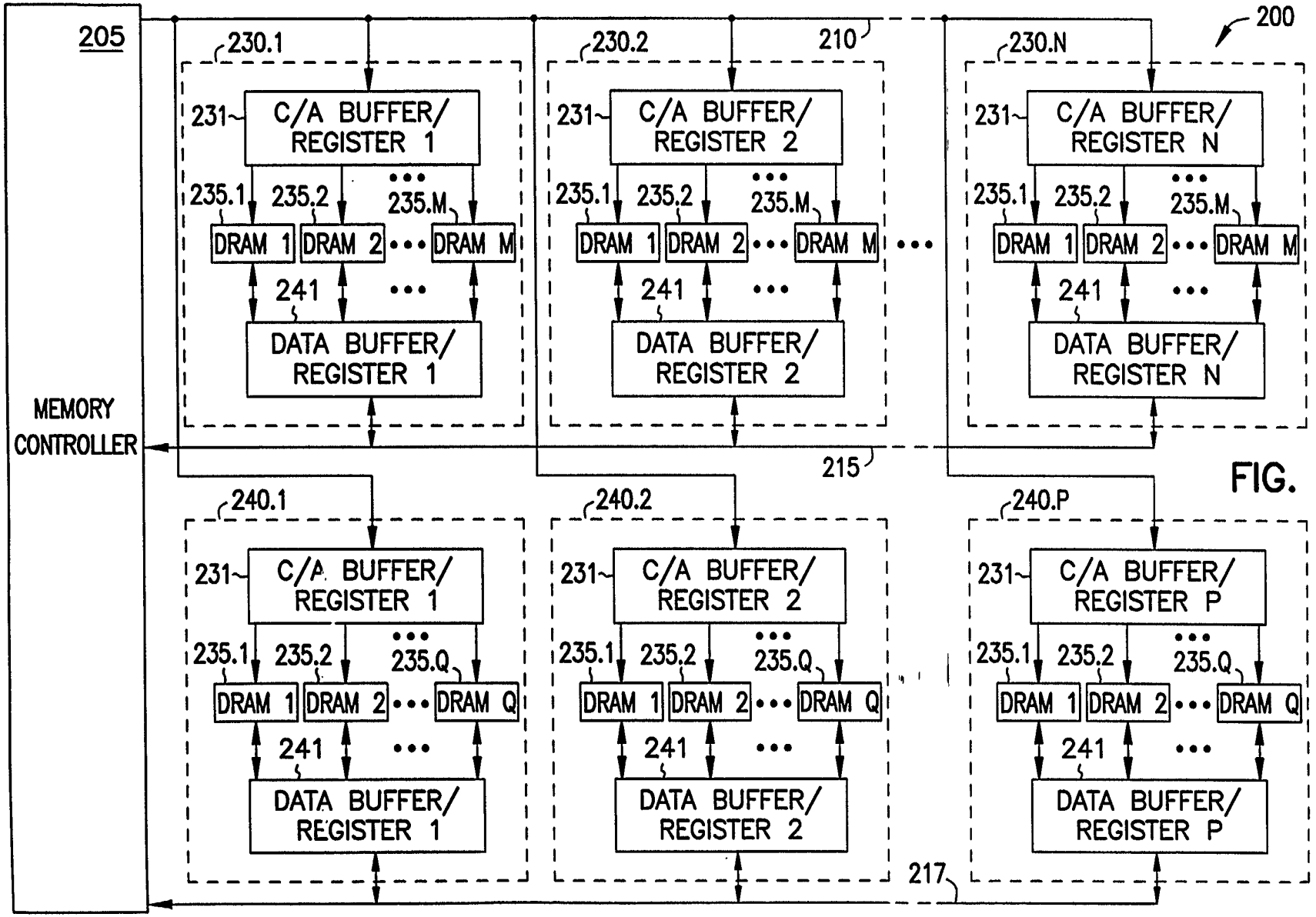

FIG. 2

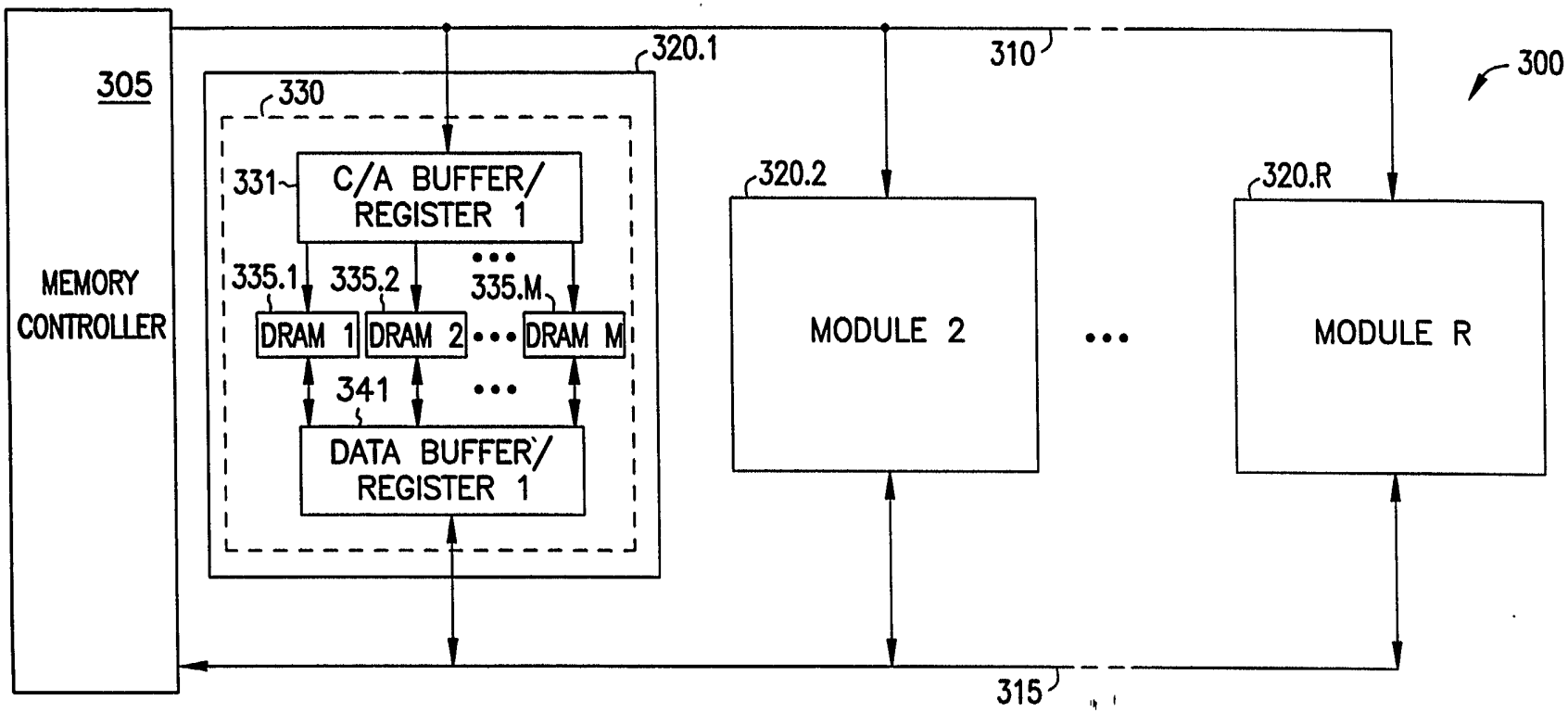

FIG. 3

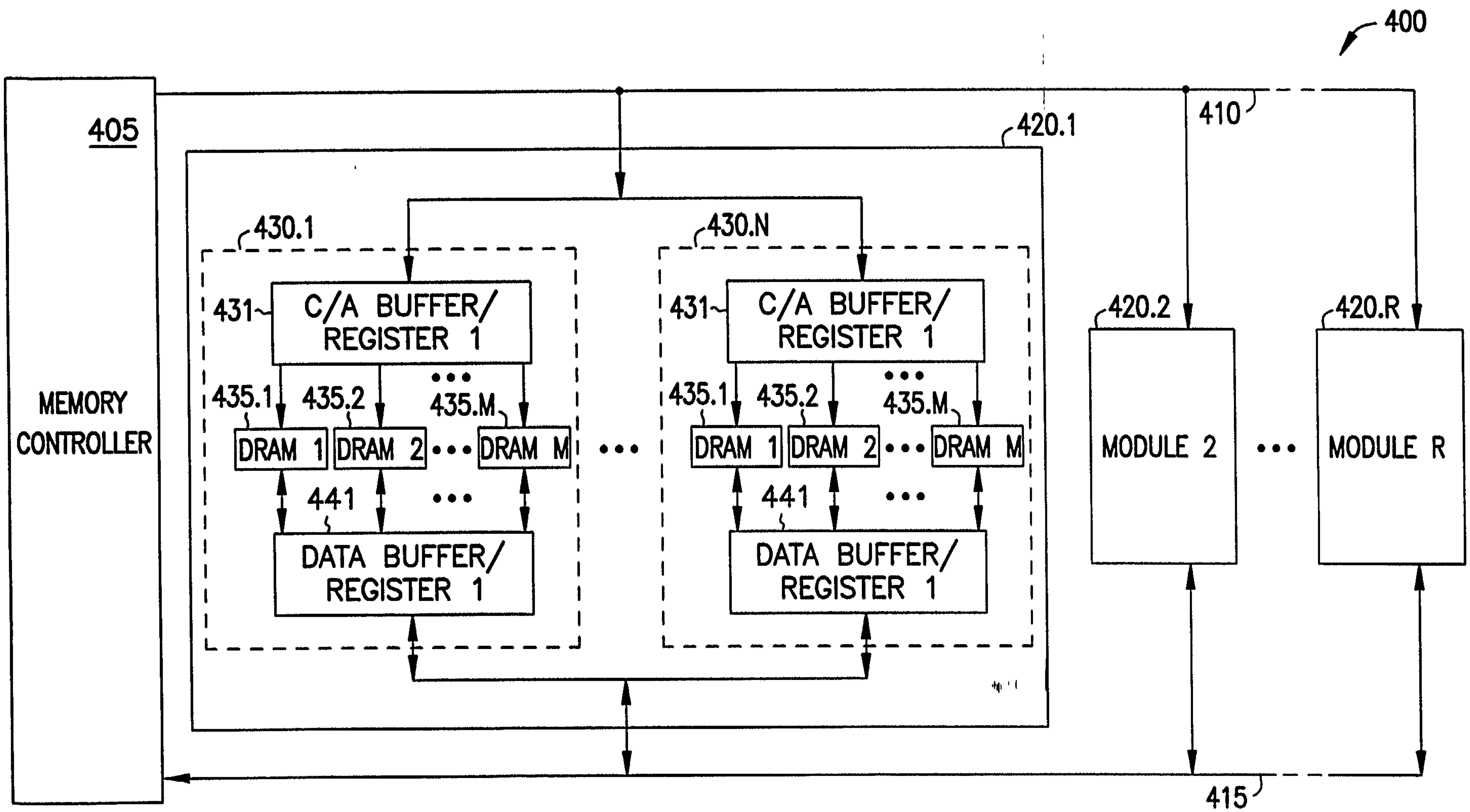

FIG. 4

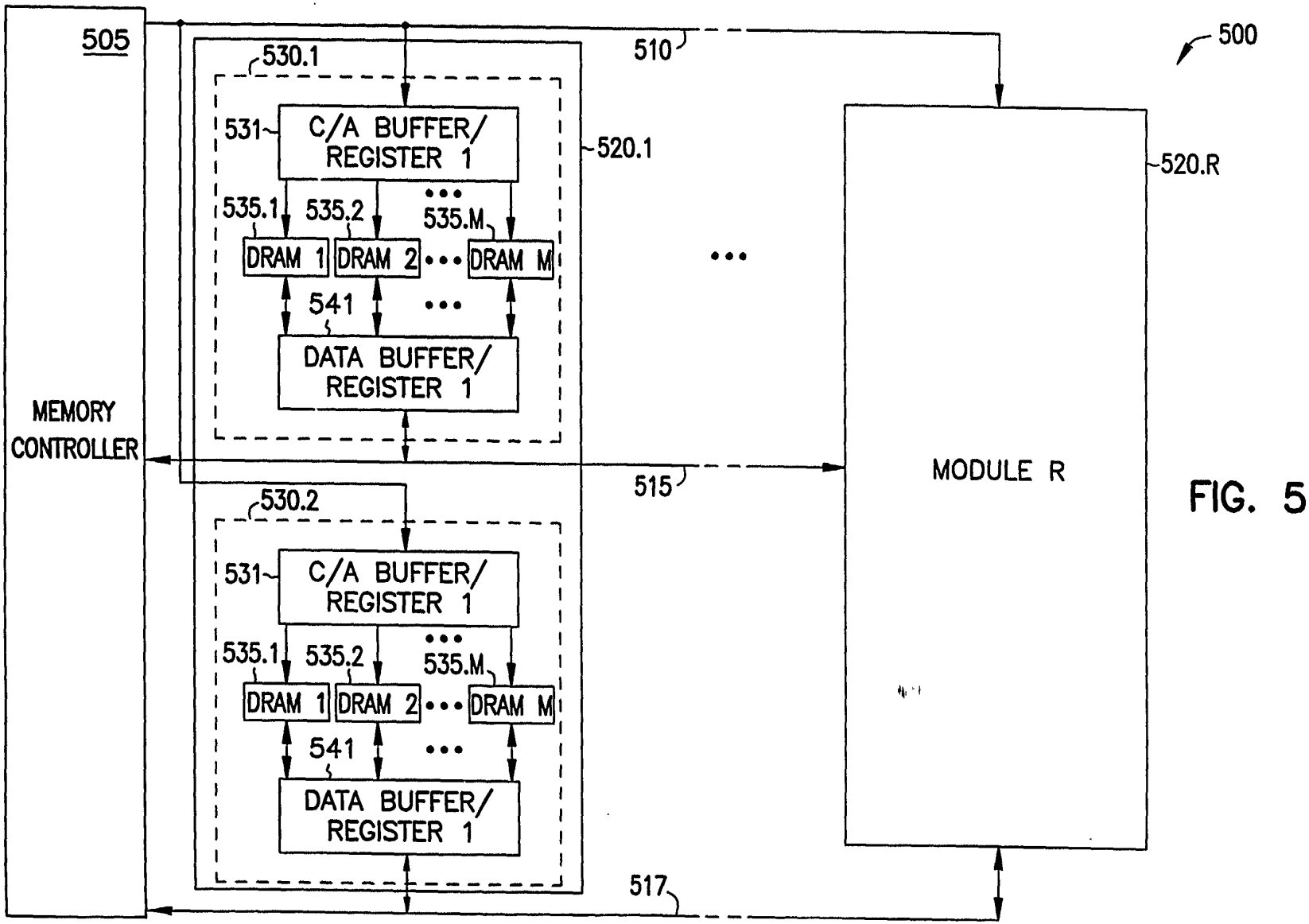
505
MEMORY CONTROLLER
530.1
531
C/A BUFFER/ REGISTER 1
535.1
535.2
535.M
DRAM 1
DRAM 2
DRAM M
541
DATA BUFFER/ REGISTER 1
520.1
510
500
520.R
MODULE R
515
530.2
531
C/A BUFFER/ REGISTER 1
535.1
535.2
535.M
DRAM 1
DRAM 2
DRAM M
541
DATA BUFFER/ REGISTER 1
517

FIG. 5

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg. No. 39,610	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Billig, Patrick G.	Reg. No. 38,080	Forrest, Bradley A.	Reg. No. 30,837	Lynch, Michael L.	Reg. No. 30,871
Billion, Richard E.	Reg. No. 32,836	Harris, Robert J.	Reg. No. 37,346	Pappas, Lia M.	Reg. No. 34,095
Brennan, Thomas F.	Reg. No. 35,075	Holloway, Sheryl S.	Reg. No. 37,850	Schwegman, Micheal L.	Reg. No. 25,816
Clark, Barbara J.	Reg. No. 38,107	Klima-Silberg, Catherine I.	Reg. No. 40,052	Slifer, Russell D.	Reg. No. 39,838
Dryja, Michael A.	Reg. No. 39,662	Kluth, Daniel J.	Reg. No. 32,146	Viksnins, Ann S.	Reg. No. 37,748
Embretson, Janet E.	Reg. No. 39,665	Lemaire, Charles A.	Reg. No. 36,198	Woessner, Warren D.	Reg. No. 30,440
Farney, W. Bryan	Reg. No. 32,651	Litman, Mark A.	Reg. No. 26,390		

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/ firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: K J L Date: 6/23/97
Kevin J. Ryan

Full Name of inventor:
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Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.